

NETHRA® AM2045™ MPPA

Asynchronous, Scalable, Massively Parallel MIMD (Multiple Instruction Multiple Data) Array

The NETHRA® Am2045 massively parallel processing array (MPPA) provides, in a single chip, up to 4.8 GFLOPS (non-IEEE single-extended floating-point). The Am2045 uses Smart Channels, a patented self-synchronizing, switched fabric which eliminates both high-speed interconnects and complex system-level state machines, enabling faster development.

Applications

The Am2045 is ideal for high-performance applications such as video processing : codecs, transcoding, transrating filtering, scaling, standards conversions, de-interlacing, 3D de-noising, image stabilization, and security analytics. It excels in signal processing applications such as medical imaging, machine vision, image enhancement, LTE or WiMax baseband, FEC, voice, radar, sonar, soft radio, test and measurement, and industrial inspection.

Benefits

Benefits of the Am2045 include a 5 to 20x performance advantage over high-end 90 nm DSPs and faster project time-to-market. The Am2045 is **fully or partially field-programmable in milliseconds**. Existing software library objects easily integrate with the proprietary objects you create. Memory includes 8 2-KB SRAM blocks per brick, plus dedicated memory for each processor; for data or instructions.

Number of bricks	# of RISC	# of μ eng	Mbits SRAM	tera OPS	GMACS 16x16-32-bit	Est. Watts
Am2045	336	8	7.14	1.03	50	6-16

On-chip Interconnect

Each switched interconnect channel operates asynchronously at 9.6 Gbps, with virtual channel support. The bi-section BW across the Am2045's mid-line totals almost 90 GBps, enabling massively parallel signal processing computation.

Available software libraries include component modules for advanced video codecs (deblocking, motion estimation and compensation, DCT, IDCT, VLC, intra-prediction, scaler, de-interlacer), and AVC-intra, VC-3 (DNxHD), and DVCPRO-HD.

Coming soon: video and image processing libraries such as H.264, MPEG-2, XDC-HD/EX, HDV, and other proven video codec formats supplied by Nethra and by third-party software partners.

Specifications

- Thermally enhanced flip-chip BGA: 31x31x3.2 mm, 896 balls, 1 mm pitch, RoHS compliant
- Temperature range: Tj = 0° to 85° C, Industrial range available
- Power: up to 15 W, 1.2 V Core voltage, 1.8 V and 3.3 V Ios

Availability: Contact Nethra

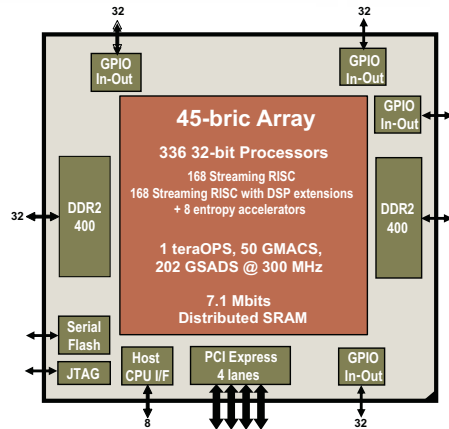


Figure 1. Am2000 teraOPS-class Chip Diagram

Features

- 336 fixed-point, 32-bit RISC processors containing 672 ALUs, in a tiled array of 42 bricks. Each RISC-bric: 4 streaming RISC processors (SR), 4 streaming RISC processors with DSP extensions (SRD) operating at up to 300 MHz. 2 DDR-dedicated bricks, 1 special entropy brick with 8 CABAC accelerators.
- SRs and SRDs include dual 16-bit operations and quad 8-bit operations for executing, looping, receiving input, and sending output all in one cycle, three ALUs including a barrel-shifter, multiplier, and single-cycle sum of absolute differences (SAD).
- SRs: compact processors for tasks such as steering data-streams or data preparation, enabling consistently high SRD throughput.
- Multiplication support: 32x32-bit with 64-bit accumulation, dual 16-bit with dual 32-bit results.

Freedom and Scalability for System Architects

- Pure software design - no hardware design, timing convergence, error-prone task scheduling: Use a standard language in a hierarchical block diagram.
- Massively parallel programming: scalable and hierarchical with and across devices.
- Well-suited to applications with both high-computation throughput and complex MIMD/SIMD data and control.
- Ability to program the most complex, irregular programs such as H.264 deblocking module with feedback loops, branching, and compute timing that all vary widely with data
- Software objects strictly encapsulated, offering timing and placement independence enabling improved validation code re-use. Software tools are easier to develop and use.
- Easily balances parallel workloads for high computing resource utilization. Synchronizing parallel computation streams supported in hardware.

Robust External IO

- Primary IO: 4 32-bit GPIOs partition into 16-bit, single-bit, and multi-bit use, aggregate bandwidth 13 Gbps from 128 bits.
- GPIO support for glueless connection to HD-SDI, DVB-ASI SERDES chips, ADCs, DACs, FPGAs, and more.
- Up to 2 discrete 16 bit DDR2-400 devices per 8 port 32-bit IF, 3.2 GBps peak BW. DIMMs not supported.
- Configuration via PCIe in < 100 ms, host interface, serial Flash, or JTAG.

	PCIe Lanes	DDR2	GPIO-32/16b	Host	JTAG	Flash
Am2045	4	2	4/8	1	1	1

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